RF ANALOG IC DESIGN

JUNE 20 – 24, 2011

The course will discuss the most important problems facing analog RF IC designers and their solutions on an advanced level. Among others, the course covers power amplifiers, up and down converters, high speed frequency synthesizers and fractional PLLs, direct conversion radio transceivers, CMOS LNAs and mixer design. The course will also discuss MOS transistor modeling for RF circuits, practical design constraints, passive components and ESD protections in RF circuits.

This course is accepted by the doctoral school of the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland. PhD students can be granted 3 ECTS credits after evaluation based upon a paper or an oral test on a theme to be agreed with the course program board. The course fulfills all the criteria imposed by the FP7 EURO-DOTS program, and has been provisionally granted the EURO-DOTS label. PhD students fulfilling the requirements can apply for scholarship. Details on the FP7 EURO-DOTS program, program, these requirements and the application procedure can be found on www.eurodots.org.

PROGRAM

Monday, June 20th 2011

8h30-12h00 am
Complex Circuits for RF Signal Processing (Andy Teetzel)

An intuitive introduction to the fundamentally complex nature of radio circuits and systems. Relevancy to modern communication systems is established by comparing and contrasting "real" and "complex" circuits, signals, modulation, and noise. Design example: circuit design and layout of an accurate and stable broadband IQ modulator RFIC. Analysis of linear and nonlinear distortions on different modulation formats, including a simple and useful graphical analysis technique.
1h30-5h00 pm
*CMOS Power Amplifiers* (Ali Hajimiri)

**Tuesday, June 21st 2011**

8h30-10h00 am
*CMOS Down Converter Mixers* (Michiel Steyaert)


10h30-12h00 am
*CMOS Up Converter Mixers* (Michiel Steyaert)

Quadrature upconverters. Basic mixer structures, linear differential transconductance topologies, single ended circuits and preamplifier buffer stages. Design example of broadband CMOS transmitter circuit.

1h30-5h00 pm
*MOS Transistor Modeling for RF IC Design* (Christian Enz)

Evolution of CMOS technologies: process scaling, low-voltage constraint. Small-signal modeling: long-channel intrinsic small-signal parameters, transcapacitances, short-channel effects, extrinsic components (junction capacitances, series resistances, overlap capacitances), intra-device substrate coupling, y-parameters, ft and fmax, NQS versus QS, noise in short-channel devices. RF measurements and parameter extraction: S-parameter measurement, deembedding, extraction methodology, noise measurement, noise parameter extraction, noise deembedding.

**Wednesday, June 22nd 2011**

8h30-12h00 am
*High Speed Synthesizers for Communications* (John Cowles)

Fractional-N synthesizers are becoming the dominant choice for communications systems for a variety of reasons that depend on the application. The need for lower phase noise, faster settling and
fine frequency resolution have elevated the interest in Fractional-N synthesizers over the traditional Integer-N approaches. The lecture will focus on the fundamental advantages and challenges with using Fractional-N synthesizers in cellular, satellite and cable application.

1h30-5h00 pm

_Fractional-N PLLs for Frequency Synthesis (Ian Galton)_

This lecture explains the extension of integer-N PLLs to fractional-N PLLs for both fine tuning resolution and in-loop VCO modulation. It presents an overview of modulus quantization noise shaping techniques, tradeoffs associated with quantization noise shaping order and PLL loop bandwidth, non-ideal effects of particular concern in fractional-N PLLs such as charge pump nonlinearities and data-dependent multi-modulus divider delays, techniques for increasing loop bandwidth, simulation techniques, and case studies of example circuits and applications.

Thursday, June 23rd 2011

8h30-12h00 am

_CMOS LNA and Mixer Design (Behzad Razavi)_

RF receiver front ends must deal with LNA and mixer design while balancing noise figure, linearity, input matching, and gain. This lecture presents various narrowband and broadband LNA and mixer topologies and their design trade-offs. Examples from the state-of-the-art are also described. A step-by-step LNA/mixer design example in 65-nm CMOS technology is presented.

1h30-3h00 pm

_Direct-Conversion Radio Transceivers (Frank Op’t Eynde)_

The Direct-Conversion transceiver principle offers the advantages of a high degree of integration, low overall system cost and low power consumption. However, the principle is difficult to implement, due to practical design limitations. In this lecture, the principle and the practical implementation of the Direct-Conversion technique is discussed.

3h30-5h00 pm

_Practical Design Constraints for RF ICs (Frank Op’t Eynde)_

This lecture focusses on the practical aspects of RF Integrated Circuit design. Special attention will be payed on the technology choice, on transistor-level design aspects and on secondary effects such as crosstalk. The problems will be discussed by means of real design examples.
Friday, June 24th 2011

8h30-12h00 am
Passive Components and RF IC Design (John Long)

Modeling, simulation, physical layout and design of monolithic passive elements for RF and high-speed applications. Circuit models for RLC components, interconnect wiring and other distributed parameter passive elements, such as transformer baluns. Simulation of passive components with traditional IC simulation tools such as SPICE and other RF simulators (e.g., Agilent-ADS and Microwave Office). The limitations and advantages of on-chip passives to the circuit designer at microwave frequencies are described using typical RF IC circuit applications.

1h30-3h00 pm
ESD Protection and Packaging of RF Circuits (John Long)

ESD input circuit design for narrowband and broadband RF circuits, ESD power clamps, co-synthesis of ESD and RF input matching circuits, ESD testing methods. Electrical characteristics of plastic IC packages and package characterization techniques. Modeling and SPICE compatible circuit models of packages for RFIC applications, such as flatpack, ball grid array and flip chip.

WHO SHOULD ATTEND

The prerequisite for the course is a basic knowledge of semiconductor devices and circuits. It addresses the training needs of all electrical engineering community involved in microelectronics and nanoelectronics.

PhD students and members of academic institutes will particularly benefit from an update information for their current research and teaching. This course is intended for any IC design engineer already working in academia or semiconductor industry, technical supervisors, managers and directors working in, or having responsibilities for:

- IC design, layout and characterization
- Research and development
- Decision making for technology choice and architectures
- Projects completion
- Teaching

The course aims to cover a broad view on the subject, from short introduction to an in-depth knowledge and to practical aspects and hints, which can be applied immediately
after the course. This is why this course will have special appeal to different level of expertise, from beginners to advanced specialists in the field.

**COURSE LOCATION**

The course will take place at the premises of the Federal Institute of Technology (EPFL), Lausanne, Switzerland.
Route description: http://www.mead.ch/info-ch/course-venue_ch.htm

**FEES AND REGULATIONS**

The fee of EUR 2,100 includes all lectures, a complete set of course notes on electronic format, lunches and two daily coffee breaks. One social evening will be organized for all attendees and instructors of the course. The social evening is usually held on the Wednesday evening.
Discounted fee for PhD students: **EUR 1,000**.
Registration deadline: **May 20, 2011**.
Payment deadline: **June 10, 2011**.

Hotel accommodations and meals other than lunches are not included in the course fee.
Mead reserves the right to cancel the program up to one month before the start of the course and its liability is limited to a full refund of the course fee.

Fees will be fully refunded if a cancellation is received by the payment deadline. No refund will be issued for cancellation notices received after this date. Registration fees may be transferred to an alternative attendee or used to pay for participation in a future MEAD course. Unpaid registrants are responsible for fees unless a cancellation is received by the deadline for payment. All reimbursement will incur a 10% fee per course.

For any further information or to contact us please see our web site: [www.mead.ch](http://www.mead.ch)